

AUTONOMOUS END SEMESTER EXAMINATIONS – DECEMBER 2024 TIME TABLE
ME (VLSI Design) Programme (2024 Batch)

Timings FN: 09.30 AM – 12.30 PM

Semester - I

Date / Day	Session	Course Code / Course Name
03.01.2025 Friday	FN	23VLR102 Computer Aided Design for VLSI Circuits
04.01.2025 Saturday	FN	23VLR103 Advanced Digital System Design
06.01.2025 Monday	FN	23VLR104 Testing of VLSI Circuits
07.01.2025 Tuesday	FN	23VLR105 Advanced Computer Architecture and Parallel Processing
08.01.2025 Wednesday	FN	23VLR106 Digital Signal Processing Integrated Circuits
09.01.2025 Thursday	FN	23MRM101 Research Methodology and IPR



T. K. Srinivasan
9/10/2024

CONTROLLER OF EXAMINATIONS

Copy to: The Principal
The Director – KTA
The Dean – Academics
The Head (ECE) – To inform the Students
Exam Cell
Office
Notice Board
File